REMARKS

Claim 1 is revised to correct the spelling error noted by the Examiner. Claim 4 is revised to remove the "preferably" limitation, a possible source of indefiniteness. New Claim 12 is added to recite that limitation. Claim 11 is amended to depend from Claim 5, providing explicit antecedent basis for the central and the upper wiring levels. Claims 1-12 remain, with no claim previously allowed.

Claims 1 and 9 were rejected as anticipated by *Hill* (US 6,028,348). The applicant respectfully traverses that rejection.

A novel aspect of the present invention is an integrated circuit arrangement in which a metallization layer comprising a metal contact of at least one active component is formed to be one of the wiring levels, in particular a lower one of the wiring levels. Please see the specification at page 1, lines 22-30 and page 4, lines 5-11. With this novel structure, one wiring level, namely the one that would have to connect the contact of the active component to other components, can be saved. This has the advantage of allowing more cost-effective production of the integrated circuit with less expense, and of improving the degree of integration of the integrated-circuit arrangement.

The rejection of Claim 1 characterizes *Hill* as disclosing a metallization layer comprising a metal contact 414 formed as a lower one of the wiring levels (citing 414 as a wiring level). However, a close reading of *Hill* fails to show anticipation of a metallization layer comprising a metal contact of at least one active component formed to be a lower one of the wiring levels, as required in the combination of Claim 1.

Hill does disclose integrated circuits with multilevel wiring structures, which the present applicant recognizes as prior art (page 1, lines 13-18). *Hill* also describes in

detail the processing steps for fabricating the different contacts to the active component, such as the emitter contact (column 3, lines 54-58), the base (column 4, lines 11-15), and the collector contact (column 4, lines 25-30). However, none of these contacts in *Hill* acts as a wiring level, i.e., a conductive layer, which forms the wiring for connecting different components of an electric circuit.

In *Hill*, any wiring connecting the active component to other electronic components on the integrated circuit is either formed through gold-plated vias 630 (column 7, lines 28-30; Figs. 6b and 6c) and the metal films 644 (column 7, lines 48-50; Fig. 6c) or through air bridges. Both of those connection structures in *Hill* are formed by additional processing steps after the contacts to the active component have been created. One example is shown in Fig. 6c in connection with column 7, lines 44-50, where the base contact 606 (see also Fig. 6b) of the transistor (HBT) is connected to the resistor 636 through the gold plating 630 and the metal film 644. Another example is shown in Fig. 7, where the emitter of the HBT is connected to a capacitor plate 708 through an air bridge.

None of the wiring levels described in *Hill* is formed by creating the contacts to the active components. That is, none of the metallization layers forming the wiring levels in the integrated circuit of *Hill* comprise any of the metal contacts of the active component. Accordingly, *Hill* does not disclose anything relevant to the present claimed invention, beyond the prior art already described by the applicant in the present application. For those reasons, Claims 1 et al. are novel over *Hill*.

Claim 3 is rejected under 35 U.S.C. § 103(a) as unpatentable over *Hill*. The applicant respectfully traverses this rejection. Dependent Claim 3 further characterizes the circuit arrangement of Claim 1 in that an electric resistor is formed in the lower

wiring level by means of an interruption in the metallization layer. The rejection mentions *Hill's* resistors 702 (shown in Fig. 7). However, *Hill* fails to disclose the basic concept of the present invention recited in parent Claim 1, as pointed out above. Moreover, nothing in *Hill* would have suggested to one of ordinary skill an integrated circuit arrangement characterized by a metallization layer comprising a metal contact of at least one active component formed to be a lower one of the wiring levels. Accordingly, Claim 3 would not have been obvious to one of ordinary skill in view of *Hill*, notwithstanding the disclosure in that reference of a resistor in an integrated circuit.

Claims 2 and 4-8 are rejected as unpatentable over *Hill* in view of *Ko* (US 2001/0053840). *Ko*, the secondary reference, is cited for teaching that a small dielectric constant below 3 is preferred. However, as discussed above with respect to the rejection of Claim 3, nothing in *Hill* would have suggested to one of ordinary skill an integrated circuit arrangement including the novel limitation recited in parent Claim 1. *Ko* does not supply that missing teaching and was not cited for that purpose. Accordingly, Claims 2 and 4-8 are patentable over *Hill* in view of *Ko*.

Claim 10 was rejected as unpatentable over *Hill* in view of *Ko*, further in view of *Baba* (US 6,853,054). *Baba* is cited as disclosing a microstrip conductor formed by means of various wiring levels in a semiconductor device. However, neither *Hill* nor the other referenced applied in this rejection discloses or suggests the novel elements set forth in parent Claim 1. Accordingly, Claim 10 is patentable over those references.

Claim 11 is rejected as unpatentable over *Hill* in view of *Shimamoto* (US 6,683,260). *Shimamoto* is cited as disclosing a waveguide in a multilayer wiring board. However, the applied art fails to disclose or teach an integrated circuit arrangement

having the novel elements set forth in parent Claim 1, as discussed above. Accordingly, Claim 11 defines an integrated circuit arrangement that would not have been obvious to one of ordinary skill in view of the cited references.

The foregoing is submitted as a complete response to the Office action identified above. The applicant submits that the present application is in condition for allowance and solicits a notice to that effect.

Respectfully submitted,

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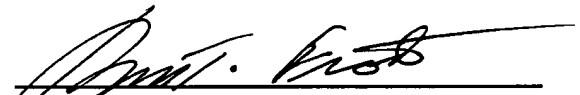

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